Thermo-Mechanical Analysis of Flexible and Stretchable Systems

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Abstract

This paper presents a summary of the modeling and technology developed for flexible and stretchable electronics. The integration of ultra thin dies at package level, with thickness in the range of 20 to 30 µm, into flexible and/or stretchable materials are demonstrated as well as the design and reliability test of stretchable metal interconnections at board level are analyzed by both experiments and finite element modeling. These technologies can achieve mechanically bendable and stretchable subsystems.

The base substrate used for the fabrication of flexible circuits is a uniform polyimide layer, while silicones materials are preferred for the stretchable circuits. The method developed for chip embedding and interconnections is named Ultra Thin Chip Package (UTCP). Extensions of this technology can be achieved by stacking and embedding thin dies in polyimide, providing large benefits in electrical performance and still allowing some mechanical flexibility. These flexible circuits can be converted into stretchable circuits by replacing the relatively rigid polyimide by a soft and elastic silicone material. We have shown through finite element modeling and experimental validation that an appropriate thermo mechanical design is necessary to achieve mechanically reliable circuits and thermally optimized packages.

1. Flexible Electronics

Flexible substrates are often an interesting alternative for replacing the rigid printed circuit boards (PBC) because of its lightweight, flexibility and in many cases, a higher mechanical reliability due to its inherent ability to deform. In order to achieve this flexibility, thinned dies in the order of 10 to 60 µm are embedded in the inner layers of the flexible boards.

One of the most common integration approaches is to connect, with flip chip technology, the dies to the circuit printed wires. However, some known issues from this approach are the impossibility of testing the dies before embedding, the high precision requirements for the placement of the bare die and the need for very fine pitch flexible printed circuit compatible with the pad pitch of the embedded chip. Another approach is to place the die in an interposer that allows, among other advantages, the possibility to test the chip before embedding and provides a fan out, eliminating in this way the need of high density PCB's and the high precision placement [1].

This novel packaging concept, named Ultra Thin Chip Package (UTCP), is based on the concept of embedding ultra thin chips, with thicknesses below 30 µm, in between two layers of polyimide, resulting in a chip package with a total thickness of only 50 to 60 µm. This package can be assembled on PCB or flex, or can be embedded in a stack of PCB layers. Details of the process flow are described in detail in [2], [3].

An example of the UTCP package and the metallization is shown in Figure 1. The metallization includes a small fan out of the 64 die contacts to a 9x9 mm^2 package with a pitch of 500 µm. The larger fan out include contacts of 650x1300 μm^2 forming a package of 30x30 mm^2. The outermost contacts can be used, for instance, to connect the integrated microcontroller for programming and testing. The inner contacts are used for embedding the UTCP package in multilayer flex boards. In this image, an SMD resistor and a LED are mounted on top of the package for visually demonstrating the functionality after processing. The integration of this package in a wireless ECG system has been demonstrated in [4], [5], [6].

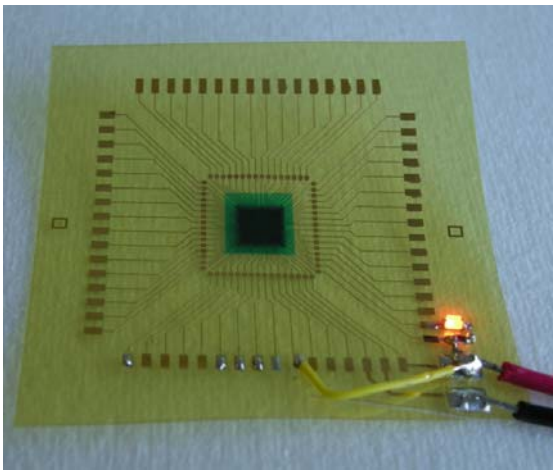

Figure 1. UTCP package of MSP430F149 microcontroller

Thin chip stacks in flexible packages

Extreme miniaturization can be achieved by embedding ultra-thin dies (between 10 to 20 µm) in a dielectric material and afterwards using 3D interconnections. Besides the advantage of saving space, die stacking may also result in a better electrical performance, because of the shorter interconnections between circuits.

Stacking of thin dies using UTCP technology provides large benefits in electrical performance, density, weight and even allows some mechanical flexibility which is a unique property for a stacked die solution. However, the thermal resistance and the thermally induced mechanical stresses during processing need to be taken into consideration for this packaging concept and therefore require an optimization of the design based on FEM simulations.

Thermal analysis

In the thermal simulation study, the objective is to get a first order calculation of the thermal resistance of the stacked package. The thermal resistance is expressed as °C/W and is a measure for its performance to remove heat from the die to the environment. The considered stacked package, based on IMEC's UTCP technology, consists of two dies in between a thin film laminated structure. In first instance, only the thermal resistance of the package itself is considered. The solder ball pads are assumed to be the reference temperature (which is set to 0C°). The heat exchange through natural convection over the surface is neglected as the outside flex material is a poor conductor and the total area is also small.

A 3D Finite Element Model (Figure 2) has been built including two silicon dies with 20 µm thickness. Also the copper tracks towards the second level bond pads were modeled in detail as the copper metallization will be the main pad for heat transfer through the package. The thermal conductivity of copper is about three orders of magnitude higher than the dielectric and adhesive materials. The silicon is also a very good conductor, but as the dies are thinned down to about 20 µm, the spreading performance of the die itself is also lower than the one of a regular die with normal thickness (this is in particular important for local hot spots on the die, which are not considered in this study).

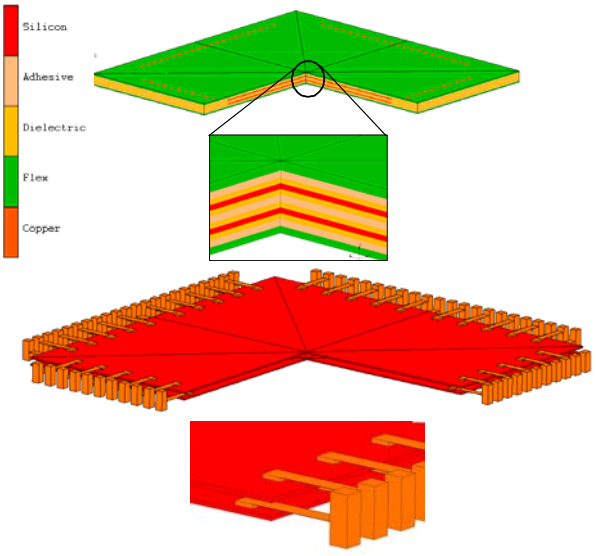

Figure 2. Finite Element Model of a stack of two UTCP packages

Figure 3 depicts the temperature distribution when 0.1 W are dissipated in each die (total power = 0.2 W). The highest temperature drop is found over the tiny copper tracks from the die to the vias. A second simulation for the same structure with a double thickness of the copper metallization (2 µm instead of 1 µm) shows that the temperature gradient over the structure is almost half of the first structure with 1 µm copper tracks. Further improvement of the design can be done by applying lots of dummy copper planes as local heat spreaders. However, this is only needed for relative high power applications (when P > 0.1 W).

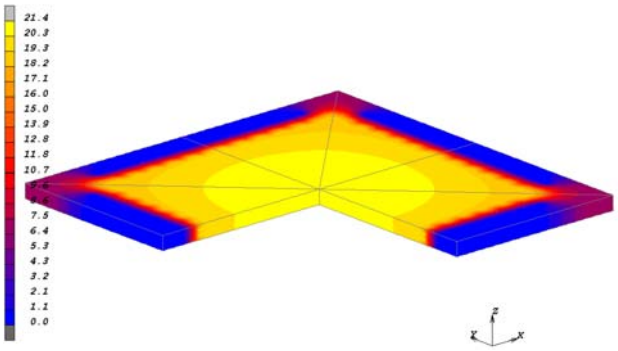

Figure 3. Temperature distribution over the stacked die package (0.1 W dissipation per die). As boundary condition, a fixed temperature of 0°C is applied to the solder pads (= bottom of the via through the stack).

Thermo-mechanical analysis

In the thermo-mechanical simulation work, the focus is on calculating the stresses and the thermal induced warpage after processing. Because the polymer materials are cured at temperatures of around 250°C, relative high stresses are induced in the "thin" dies. Moreover, as the total thickness of a UTCP is small, the stiffness of the overall structure is insufficient to overcome the strong warpage after cooling, becoming a reliability problem. Even if it is attached on a temporary carrier; a strong warpage can cause self-detachment from the carrier. An example of the warpage of the UTCP after processing, once released from the carrier, is shown in Figure 4.

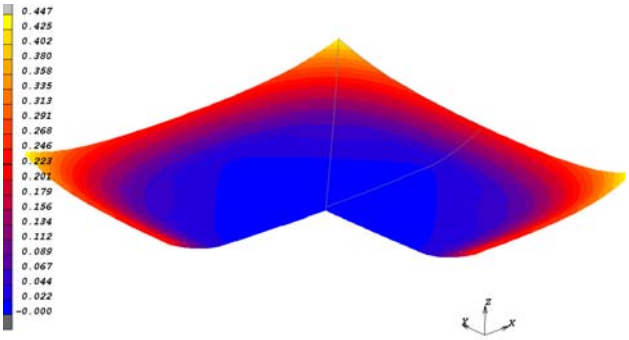

Figure 4. Warpage of one UTCP after processing

Using FEM, the optimal dielectric materials are selected in order to minimize stress and warpage of the UTCP. In future work, the thermo-mechanical study on a full stack of UTCP's will be analyzed.

2. Stretchable Electronic

The basic principle of stretchable electronics is to interconnect rigid or flexible interposers, containing the electronic components, by means of elastic electrical conductors. In order to protect the circuit from environmental factors and to provide a mechanical stability, the interposers and the interconnections are embedded into an elastic polymer.

Even though stretchable electronic technology is not as mature as the flexible circuits, many different concepts have been proposed in recent years, covering a wide range of applications with dimensions of only few hundreds of microns [7], [8] to some tens of centimeters [9], [10]. Each technology presents some advantages and disadvantages among each other, and the choice of the technology depends largely on its final application.

One concept consists in depositing a thin metal film in a pre-stretched substrate. It is reported that once the substrate is released, the metal will deform out-of-plane forming a controlled buckled structure [11]. Even though this unique design offers a controllable stretchability without losing electrical performance, it is limited to relatively small circuits and deformation of only a few percent.

A similar process technology involving an out-of-plane deformation of a thin metal has been investigated. It has been proven that while stretching a 100 nm gold film deposited on top of an elastic substrate, multiple micro cracks are formed in the metal during the stretching allowing deformations up to 50 percent [12], [13]. Drawbacks of this technique are the electrical restrictions of extremely thin metal films, the need for high cost equipment and the processing of non standard assembly technology on those substrates. Furthermore, the number of micro cracks increase as the substrate is deformed and therefore, a change in the resistance of the line is observed during the stretching. Some applications of this technology include electronic circuits used for skin electronics [14] and microelectrode arrays used for monitoring the neuron activity in the brain [15]. The choice in IMEC technology is based on the realization of high electrical performance metallic interconnections patterned as a planar 2D spring and embedded in silicone elastomers. An example of such design is depicted in Figure 5.

Depending on the desired metal track dimensions, it is possible to use either a Mould Interconnect Device (MID) technology [16], [17], or use a standard thin film technology at wafer level [18]. In the first case, the metal meanders are formed either by using electroplating, photolithography and wet etching or laser patterning [19]. In all these cases, standard rigid packages are connected with the elastic electrical interconnections using either conductive adhesives or conventional lead free SnAgCu alloys. Finally, the circuits are embedded in an elastic material such as PDMS or polyurethane. More than 100% deformation has been achieved with this technology and reliability of several thousand of cycles has been achieved [20], [21]. High density interconnections are also being investigated combining technologies such as die thinning and stretchable circuit technology. This technology named Ultra Thin Chip Flexible (UTCF) consists in embedding thin dies and metal interconnects in a polymer at wafer level, and then release them from the wafer.

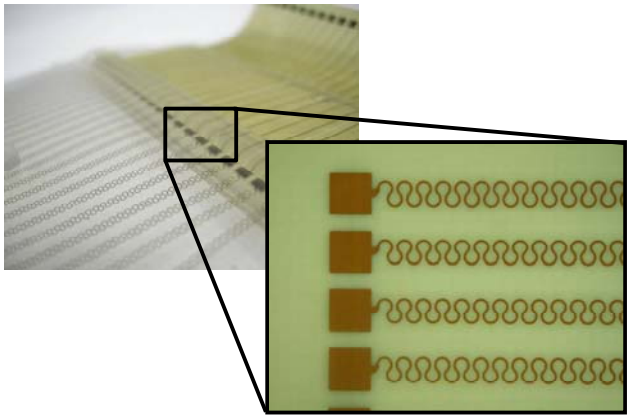

Figure 5. Stretchable copper interconnection

Wafer level stretchable circuits

High density stretchable interposers have been developed in IMEC. This technology consists in embedding a thin silicon die (below 20 µm) and the metal interconnections in a stretchable polymer. All operations, except dies transfer, are done in a wafer-level packaging process manner, allowing fast processing of a large number of dies, minimizing costs and time. Thanks to its ease of application, the metallization can be designed with complex geometries allowing some degree of stretchability. Figure 6 depicts an example of a thin embedded die and the metal interconnections before and after releasing from the wafer.

As stretchable substrate, a photo sensitive spin on silicone, WL5150, has been used because of its high elasticity and low induced stresses from the relatively low Young's modulus (<160MPa) and large elongation to break (~37%). The temperature stability of the material up to 300°C allows for further assembly while remaining under CMOS compatible process temperature (<400°C).

To allow stretchability of the package, metal interconnections have to be stretchable as well. We therefore use a specific design of metal lines with a kind of sinusoidal shape allowing to stretch them such as a 2D spring. In this design, pitch on the die is 100 µm (80 µm pads) and fanned-out to a 400 µm pitch (300 µm pads). This "large" pitch is compatible with stretchable board technologies. The dimensions on this design are typical for standard targeted applications.

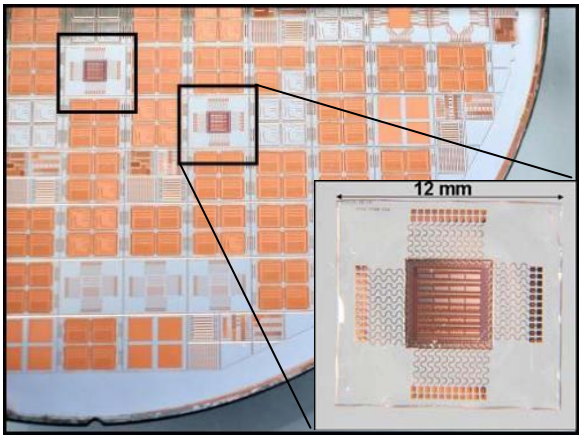

Figure 6. Thin dies embedded into dielectric and interconnected with metals before release (on wafer)

In this activity, extensive finite element modeling (FEM) is carried out in order to maximize stretchability of the overall embedded subsystem in general and of the metal interconnects in particular. As the required stretchability of these interposers will not exceed 10%, a horseshoe design is not necessary.

Figure 7 illustrate a comparison of the permanent deformation of the copper between straight lines and the meandered lined. In this case, the applied deformation in the package is 5%. As the rigid silicon chip does not elongate, the effective stretch in the copper meanders is 8.7%. As it can be seen in Figure 7, the meandered lines are more reliable than straight lines because of the lower plastic strain. Even though there is a reduction in the plastic strain of the meander line compared to the straight lines, the plastic strain is concentrated in specific zones of the curve, therefore further optimization of the transition zone from rigid (silicon die) to stretchable (copper meanders) need to be investigated. Further improvements have been observed by reducing the copper track width.

In order to keep a low electrical resistance and increase, at the same time, the stretchability of the meanders, multiple copper meanders, parallel to each other are designed as shown in figures 7 & 8.

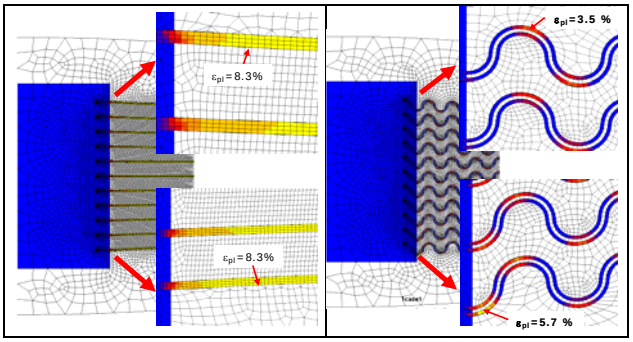

Figure 7. FEM of thin dies and metal interconnections embedded in a silicone encapsulant. Left image: straight interconnections. Right image: Double meander interconnections

In the case of multiple metal conductors forming a single line, electrical bridges are placed between the tracks in the regions where the lowest deformation is observed (Figure 8). These bridges help to keep the continuity of the lines after failing in a specific region. In other words, if a metal track fails, only one section of the line is lost (between two bridges) in electrical connection instead of the failure of the whole track. This redundancy helps to increase the reliability of the system.

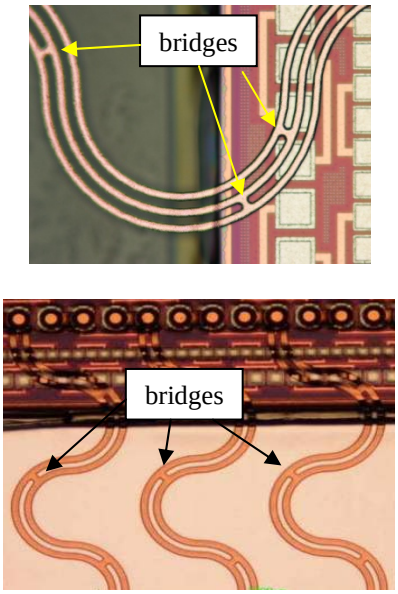

Figure 8. Stretchable metal interconnections including electrical bridges between meanders.

Board level stretchable circuits

Metal conductors are by nature only elastic for a few percent before break, therefore the design of the metal meanders is a dominant factor to give stretchability to a non-stretchable material. It has been widely used by FEM to characterize the shape of the conductors in order to allow high deformations without permanent damage. Based on these results, a horseshoe metal track shape is proposed. In this design, the stresses are distributed in a wider region instead of concentrated in the apex of the curve. The damage in the metal is significantly reduced by applying narrow metallization schemes and low elastic modulus of the substrate [16], [21]. Figure 9 shows and example of a horseshoe design. After deforming 30%, the maximum plastic strain is only 4.83%. Nevertheless, the magnitude of the stresses and the level of plastic strain are related to the stiffness of the substrate, the geometry of the meanders and the interaction with neighboring meanders.

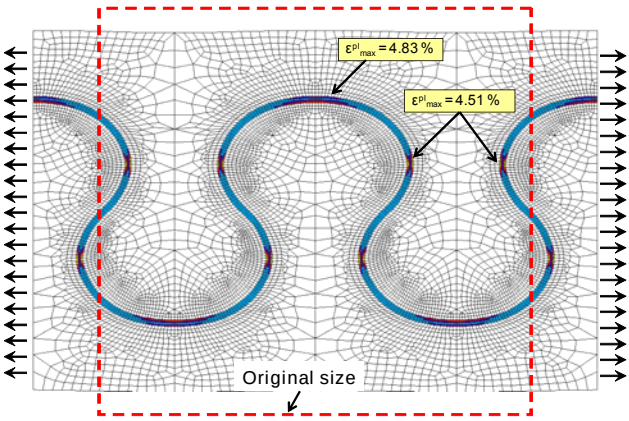

Figure 9. Equivalent plastic strain in the horseshoe design after deformation of 30%. Dashed line shows the original dimensions of the substrate.

The deformation of the interconnection lines can be different when several meanders are close to each other, or depending on the position of the lines. An example of this phenomenon is shown Figure 10. A total nominal deformation of 25% is applied in a uniaxial manner. In the entire test sample we can observe three regions of interest: the clamping zone, where no in-plane deformation is applied; a transition zone, following the rigid clamp, where a complex deformation is presented, and a stable and homogeneous region where all the meanders deform in the same mode.

From the reliability point of view, the transition zone is the critical region; because of the different deformation modes are observed and the maximum elongation of the meanders is observed. Some of the factors affecting this zone:

- As no contraction is allowed in the "Y" direction, the substrate and copper meanders in this region are deformed as a planar extension test and shows slightly higher damage when compared to the uniaxial tensile test.
- The outermost meanders are bended and stretched, while the centre meanders are only stretched. This means that the total deformation of the outermost copper meanders is higher (lower reliability) than the deformation of the central meanders. This effect is illustrated in Figure 11.
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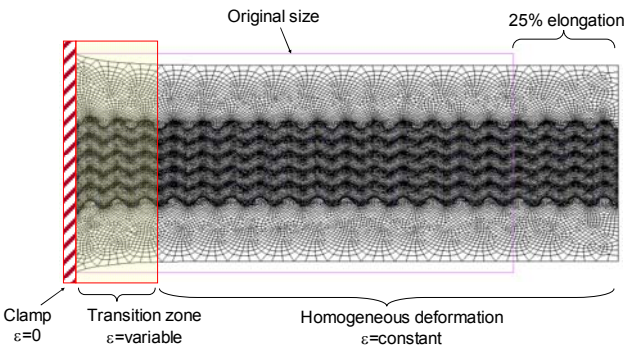

Figure 10. Deformation of multi-line circuit

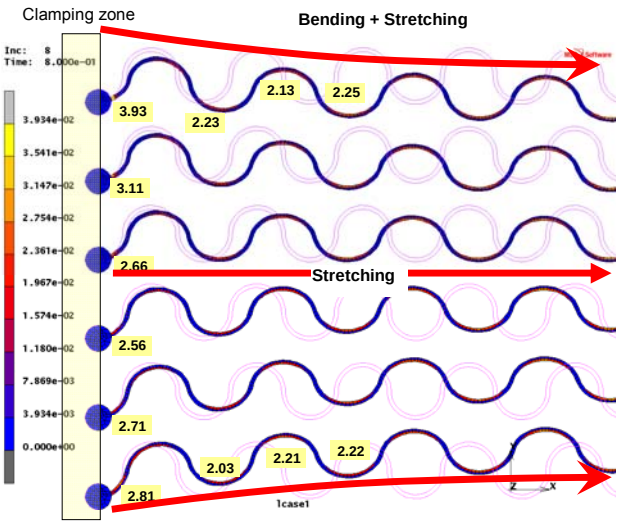

Figure 11. Equivalent plastic strain in the copper meander within the transition zone (values in %). Red curves indicate the displacement direction

In some applications, where a high density interconnections and low stretchability are required, the horseshoe design is not longer a suitable design. Due to the shape of the horseshoe, it is not possible to "stack" parallel lines; therefore the minimum pitch is governed by the amplitude of the meander. For those applications a pattern with a zigzag structure is designed as shown in Figure 12. This design, as the horseshoe, presents the characteristic that its electrical resistance is independent on the elongation before metal rupture. Stretchability beyond 40% has been demonstrated with this design [22]

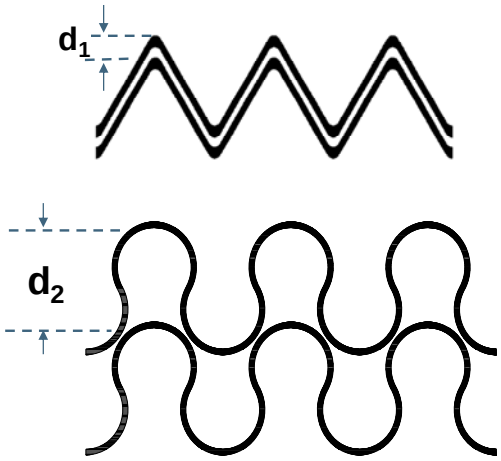

Figure 12. Schematic of the pitch comparison between zigzag and horseshoe interconnections.

Reliability and Failure Analysis

As it was discussed in previous sections, the reliability of the stretchable interconnections depends not only on the constitutive behavior of the substrate and the metal interconnections but also on the mechanical design and

the applied deformation. FEM simulations results presented here were done for a specific design and deformation and presented as the maximum plastic strain in the copper. During fatigue cycles, much smaller but periodic, elongations are applied to the circuits producing a fatigue failure of the metals. In order to model the fatigue test and estimate the fatigue lifetime, the stretchable circuit was subjected to cyclic deformations at a specific percentage and a FEM model was used to calculate the accumulated plastic strain per cycle for the same elongation. These kinds of tests were repeated for 7 different elongations going from 2.6% to 22%. In this way, we "translate" the applied strain into a damage criterion (plastic strain). If a new design is created or the thickness of the substrate is modified, we can use the FEM to calculate the plastic strain and therefore estimate the fatigue lifetime. The result of this "translation" is depicted graphically in Figure 13. In this plot, the accumulated plastic strain per cycle is the value calculated by FEM, whereas the lifetime is obtained experimentally. An equation based on the Coffin-Manson law is used to fit the data points into a correlation curve.

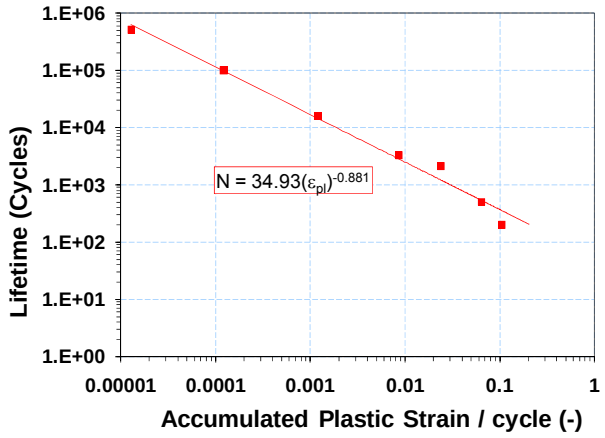

Figure 13. Fatigue lifetime of copper line versus simulated plastic strain. Copper modelled as a perfect plastic material

In order to observe the failure mechanism, a home built stage was mounted directly in the SEM in order to monitor *in-situ* the deformation mechanism of the horseshoes shaped metal tracks. The samples were specially designed, with the copper exposed in the surface of the silicone. In this way, it was possible to take high resolution images of the elastic interconnections at different phases of the deformation. Figure 14 shows a horseshoe meander deformed 100%. Several observations are done from these images. Firstly, although the copper metal is deposited in-plane, during the deformation, a combined "opening" of the horseshoe and twisting of the metal is observed giving rise to an out-of-plane deformation of the meander. This mechanism is beneficial for the reliability because it implies a lower induced plastic strain. Secondly, before the final break of the copper track, an interfacial delamination is observed, as illustrated in Figure 14. More detailed explanation of this mechanism are presented experimentally by Hsu in [22] and numerically by van der Sluis in [23]

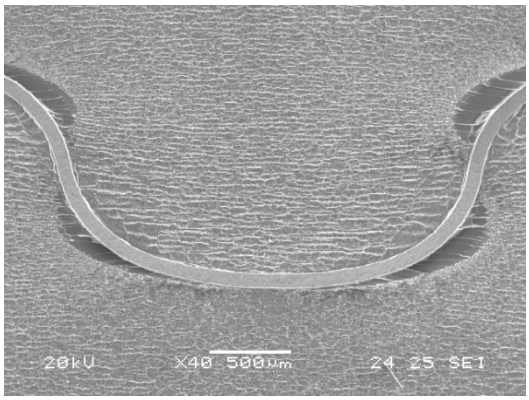

Figure 14. SEM image of a horseshoe patterned interconnect stretched 100%.

In order to understand the mechanisms leading to a delamination of the copper meanders from the silicone substrate, the interface properties were characterized by a series of peel-tests done in a uniform copper layer deposited on top of a silicone substrate. These samples followed the same process flow as the one used to fabricate the stretchable circuits. In these tests, the necessary force to peel-off the thin film from the substrate is monitored as a function of the clamp displacement and the adhesion energy is calculated from these experiments. The obtained interface parameters were used in a FEM in a form of interfacial cohesive elements located in the interface between the copper and the silicone. A model simulating the deformation of a representative horseshoe section was done. An example of this model is shown in Figure 15. The original location of the copper film is indicated as the curved thin lines on the substrate. A very good agreement between the in-situ experiment and the delamination model is observed. A detailed explanation of the peel test experiments and the FEM was presented by van der Sluis in [23]

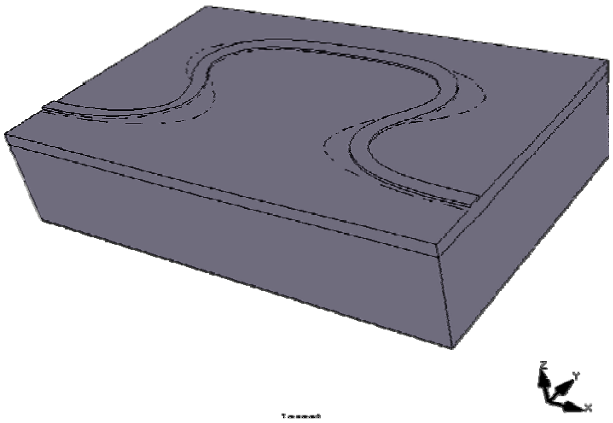

Figure 15. FEM of a 67% stretched horseshoe pattern interconnect, showing the original and final position of the copper meander.

4. Conclusions

It is believed that in future many electronic assemblies on rigid substrates will be replaced by mechanically flexible or even stretchable alternatives. The success of flexible and stretchable electronics is based in the broad number of applications where the weight, size, cost and shape among others are an asset. This paper summarizes the ongoing activities for the integration of IC at a wafer level and board level for flexible, stretchable and potentially smaller devices.

Acknowledgments

The presented work was performed in the frame of the Integrated Projects TIPS and STELLA, which are financially supported by the European Commission FP7 and FP6 programs respectively.

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